IN THE CLAIMS:

Please amend claims 1 and 7 as shown in the complete list of claims that is presented below.

1. (currently amended) A semiconductor integrated circuit having an operational mode for processing operation input data and a test mode for processing test input data, comprising:

a plurality of scan registers that are operable in response to a clock signal and a mode signal, each scan register having an output terminal, an operation input data terminal, and a test input data terminal;

a plurality of logic circuits, each having an input terminal and having an output terminal that is connected to the operation input data terminal of one of the scan registers, the logic circuits and the scan registers being connected alternately in series to form m scan chains (wherein m is an integer greater than 1), ~~each of which includes a plurality of logic circuits and a plurality of scan registers connected alternately in series, the scan registers being operated in response to a clock signal,~~ the scan chains being connected to one another in a sequence, each of the scan chains including a first logic circuit, ~~having a data input terminal,~~ a first scan register connected to the first logic circuit, ~~the first scan register having a test input terminal,~~ and a last scan register; ~~having an output terminal;~~

a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains, the serial/parallel conversion circuit converting serial test input data supplied during the test mode into parallel test input data in response to a multiplied clock signal having a frequency that is m times that of the clock signal, the parallel test input data being fed in parallel to the scan chains; and

a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains, the parallel/serial conversion circuit converting parallel data received from the scan chains into serial data in response to the multiplied clock signal,

wherein the parallel/serial conversion circuit comprises a selector that receives the clock signal and selectively outputs processed test input data from the last scan registers

of the scan chains in response to the clock signal during the test mode, and a flip-flop that receives the multiplied clock signal and latches output data from the selector in response to the multiplied clock ~~signal.~~ signal,

wherein operation input data is supplied to the sequence of scan chains via the input terminal of the first logic circuit in a first one of the scan chains in the operational mode, and

wherein the flip-flop outputs processed operation input data from the sequence of scan chains during the operational mode.

2. (previously presented) A semiconductor integrated circuit according to claim 1, further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit, the multiplication circuit receiving the clock signal and generating the multiplied clock signal based on the clock signal.

3. (previously presented) A semiconductor integrated circuit according to claim 1, wherein the serial/parallel conversion circuit includes a plurality of flip-flops connected in series, the flip-flops being operated in response to the multiplied clock signal.

4. (previously presented) A semiconductor integrated circuit according to claim 1, wherein the parallel/serial conversion circuit further includes at least one additional flop-flop that receives the multiplied clock signal.

5. (previously presented) A semiconductor integrated circuit according to claim 1, wherein each of the scan registers includes a selector and a flip-flop operated in response to the clock signal.

6. (previously presented) A semiconductor integrated circuit according to claim 1, wherein the output terminal of the last scan register of one of the scan chains is

connected to the data input terminal of the first logic circuit of another one of the scan chains.

7. (currently amended) A semiconductor integrated circuit having an operational mode for processing operation input data and a test mode for processing test input data, comprising:

a plurality of scan chains that are connected to one another in a sequence, each ~~of which includes~~ scan chain including a first logic circuit having ~~a data~~ an input terminal and an output terminal, a first scan register ~~connected to the first logic circuit, the first scan register~~ having a test input terminal and having an operation input data terminal that is connected to the output terminal of the first logic circuit, and a last scan register having an output terminal, the scan registers being operated in response to a clock signal and a mode signal;

a serial/parallel conversion circuit connected to the test input terminals of the first scan registers of the scan chains, the serial/parallel conversion circuit converting serial test input data supplied during the test mode into parallel test input data in response to a multiplied clock signal having a frequency that is substantially equal to the number of scan chains times the frequency of the clock signal, the parallel test input data being fed in parallel to the scan chains; and

a parallel/serial conversion circuit connected to the output terminals of the last scan registers of the scan chains, the parallel/serial conversion circuit converting parallel data received from the scan chains into serial data in response to the multiplied clock signal,

wherein the parallel/serial conversion circuit comprises a selector that receives the clock signal and selectively outputs processed test input data from the last scan registers of the scan chains in response to the clock signal during the test mode, and a flip-flop that receives the multiplied clock signal and latches output data from the selector in response to the multiplied clock ~~signal.~~ signal,

wherein operation input data is supplied to the sequence of scan chains via the input terminal of the first logic circuit in a first one of the scan chains in the operational mode, and

wherein the flip-flop outputs processed operation input data from the sequence of scan chains during the operational mode.

8. (previously presented) A semiconductor integrated circuit according to claim 7, further comprising a multiplication circuit connected to the serial/parallel conversion circuit and the parallel/serial conversion circuit, the multiplication circuit receiving the clock signal and generating the multiplied clock signal based on the clock signal.

9. (previously presented) A semiconductor integrated circuit according to claim 7, wherein the serial/parallel conversion circuit includes a plurality of flip-flops connected in series, the flip-flops being operated in response to the multiplied clock signal.

10. (previously presented) A semiconductor integrated circuit according to claim 7, wherein the parallel/serial conversion circuit further includes at least one additional flip-flop that receives the multiplied clock signal.

11. (previously presented) A semiconductor integrated circuit according to claim 7, wherein each of the scan registers includes a selector and a flip-flop operated in response to the clock signal.

12. (previously presented) A semiconductor integrated circuit according to claim 7, wherein the selectors of the scan registers are operated in response to a mode signal.

Claim 13-14 (cancelled).